Digital Design Lab
EEN 315 Section 3G

Lab 3
Tone Generator

Group 5
Nathan Paternoster
(Partners: Michael Finale, Daniel Bennett)

Sayan Maity, TA

University of Miami

November 1st, 2013

Abstract

In this lab we will generate a sequence of audible tones through a speaker. First, a sequence generator will be designed using medium-scale integration combinational logic (multiplexers) and D flip-flops. The sequence generator will generate a set sequence of binary-coded states. Second, a frequency (tone) generator will create a signal depending on which state the counter is outputting. The frequency generator is composed of a counter and a 555 timer in astable mode. The frequency generator will be put through a frequency divider (composed of a T flip-flop) before outputting to a speaker. We will hear a unique output frequency for each state.

Table of Contents

Overview

The circuit will be composed of two stages – a sequence generator and a frequency generator cascaded like so:

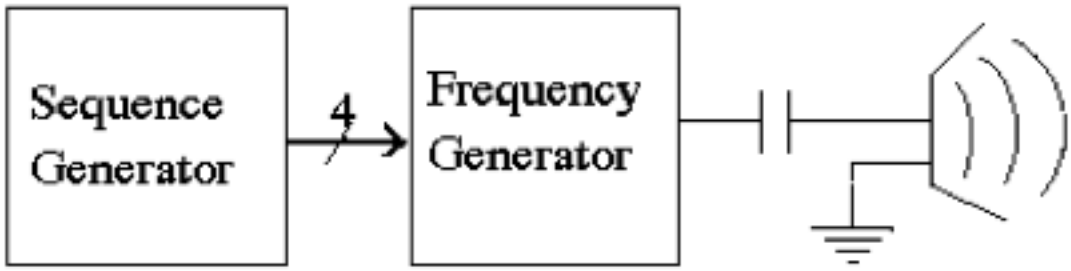


Figure 1 Block Diagram of Tone Generator

The sequence generator will be designed to run through 13 states in this order: *0, 11, 14, 13, 8, 9, 12, 3, 2, 10, 5, 6, 1, 0, etc.* Therefore it will require 4 bits to represent each state. This means there will be four 8-to-1 multiplexers and four corresponding D flip-flops.

The frequency generator will utilize a 555 timer in astable mode to provide an output signal with a base frequency of f_0 = 16kHz and a duty cycle of 60%. The four outputs of the sequence generator will be fed into a 4-bit, up/down, loadable counter. The clock of this counter will be powered by the 555 timer. If the counter receives an invalid state it will go directly to state 0. The counter will divide the frequency depending on the current state (N) according to the equation $f_N = f_0/(N+1)$. This signal outputted by the counter will be further divided using a T flip-flop. The T flip-flop will divide the frequency in half: $f_N = (1/2)f_0$. The resulting output frequency will be $f_N = f_0/(N+1) * (1/2) = f_0/[2(N+1)]$ where N is the current state. The final signal will be put through a capacitor (to remove a DC offset) and connected to a speaker.

Objectives

To demonstrate how a 555 timer may be used to generate a frequency and how a counter and a flip-flop may be used to divide that given frequency.

Equipment

Description	Chip Number	Quantity
8-line to 1-line Multiplexers	74151	4
Dual positive-edge-triggered D flip-flops	7474	2
Dual positive-edge-triggered J-K flip-flops	7476	1
Synchronous 4-bit up/down binary counters	74169	1
LM555 Timer	LM555	1
Other		
1 x 1.8kΩ Resistor, 1 x 3.6kΩ Resistor		
1 x 1nF Capacitor, 1 x 0.047μF Capacitor		

Description

The first stage of the design process will be designing the sequence generator. Step 1 will be to write the next state table based on the sequence we're given. There will need to be four total flip-flops (A, B, C, and D) to represent a state (four bits for each state). A is the most significant bit (MSB) and D is the least significant bit (LSB). Each flip-flop will be accept the output of a multiplexer (A/B/C/D) as its input and will output the next state variables ($Q_A/Q_B/Q_C/Q_D$). The four multiplexers

will be 8-to-1 MUX's and will accept Q_A, Q_B, and Q_C as their select lines. Q_D, the LSB, will be chosen to be the MUX's input variable. For step 2 we will use MUX design tables to determine the inputs to the multiplexers. All flip-flops will be connected to the same external clock.

The second stage of the design process will be designing the tone generator. A 555 timer will be setup in astable mode as given by this diagram:

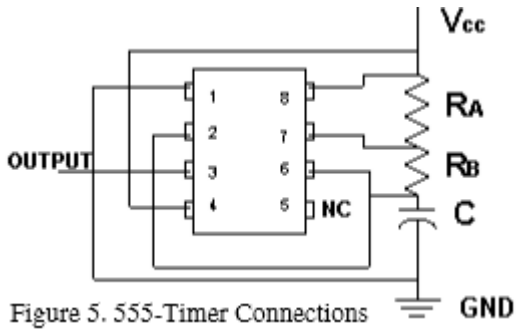


Figure 5. 555-Timer Connections

We will calculate the two resistor values and capacitor value using given formulas:

$$duty\ cycle = \frac{R_A + R_B}{R_A + 2R_B} = 60\%$$

$$0.6R_A + 1.2R_B = R_A + R_B$$

$$R_B = 2R_A$$

$$Choose\ R_A = 1.8k\Omega$$

$$R_B = 3.6k\Omega$$

$$f_0 = 16kHz = \frac{1.44}{(R_A + 2R_B)C}$$

$$C = \frac{1.44}{16k * (1600 + 2(3600))} = 10nF$$

The output of the 555 timer will be connected into the clock of a 4-bit, up/down counter. This counter will accept the outputs of the four flip-flops as its four inputs (Q_A, Q_B, Q_C, and Q_D). On the 74169 chip the $U/\overline{D}$ is set to HI, the $\overline{ENP}$ to LO, and the $\overline{ENT}$ to LO. The counter is set to count up and the $\overline{ENP}$ and $\overline{ENT}$ pins are low-enable pins.

In order to obtain the frequency division by the current state N we use the $\overline{RCO}$ and load pins as the output of the counter. Cascading the ripple carry output ($\overline{RCO}$) into a T flip-flop results in the frequency division of $f_N = f_0/[2(N+1)]$. The output of the counter will be put into the T flip-flop's clock and a logical '1' will be put into the T input. This will only allow the signal to pass every other clock pulse, effectively halving the frequency. However, we don't have a T flip-flop component available, so we must perform flip-flop conversion on a J-K flip-flop to achieve a T flip-flop. Step 3 to designing the circuit is comparing the two flip-flop's excitation tables to perform this conversion.

Finally, the output of the T flip-flop will be run through a capacitor (specified to be 0.047**µ**F) and connected to a speaker.

Specifications

Must use a minimum of 10 states for the sequence generator. Must use a 555 timer in astable mode with a duty cycle of 60% and a base frequency of 16kHz. Must use a 74LS76 J-K flip-flop to implement the T flip-flop. Must use a 0.047**µ**F capacitor before the speaker.

Design Synthesis

Step 1: the next state table. A, B, C, and D represent each bit of the present state. Q_A, Q_B, Q_C, and Q_D represent each bit of the next state. The invalid states are highlighted in green.

	PS	NS				
	ABCD	**Q_A**	**Q_B**	**Q_C**	**Q_D**	
0 =	0000	1	0	1	1	*= 11*
1 =	0001	0	0	0	0	*= 0*
2 =	0010	1	0	1	0	*= 10*
3 =	0011	0	0	1	0	*= 2*
4 =	0100	0	0	0	0	*= 0*
5 =	0101	0	1	1	0	*= 6*
6 =	0110	0	0	0	1	*= 1*
7 =	0111	0	0	0	0	*= 0*
8 =	1000	1	0	0	1	*= 9*
9 =	1001	1	1	0	0	*= 12*
10 =	1010	0	1	0	1	*= 5*
11 =	1011	1	1	1	0	*= 14*
12 =	1100	0	0	1	1	*= 3*
13 =	1101	1	0	0	0	*= 8*
14 =	1110	1	1	0	1	*= 13*
15 =	1111	0	0	0	0	*= 0*

Step 2: the MUX design tables.

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
D=0	1	1	0	0	1	0	0	1
D=1	0	0	0	0	1	1	1	0
	$\overline{D}$	$\overline{D}$	0	0	1	D	D	$\overline{D}$

Q_A

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
D=0	0	0	0	0	0	1	0	1
D=1	0	0	1	0	1	1	0	0
	0	0	D	0	D	1	0	$\overline{D}$

Q_B

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
D=0	1	1	0	0	0	0	1	0
D=1	0	1	1	0	0	1	0	0
	$\overline{D}$	1	D	0	0	D	$\overline{D}$	0

Q_C

ABC	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
D=0	1	0	0	1	1	1	1	1
D=1	0	0	0	0	0	0	0	0
	$\overline{D}$	0	0	$\overline{D}$	$\overline{D}$	$\overline{D}$	$\overline{D}$	$\overline{D}$

Q_D

Step 3: JK to T flip-flop conversion

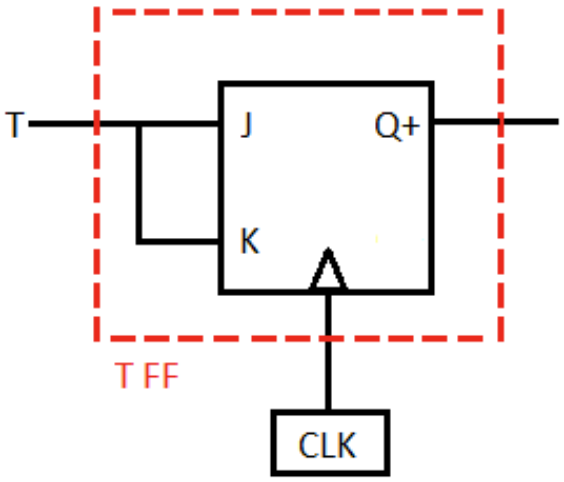
T	Q	Q+	J	K
0	0	0	0	x
0	1	1	x	0
1	0	1	1	x
1	1	0	x	1

		Q	
		0	1
T	0	0	x
	1	1	x

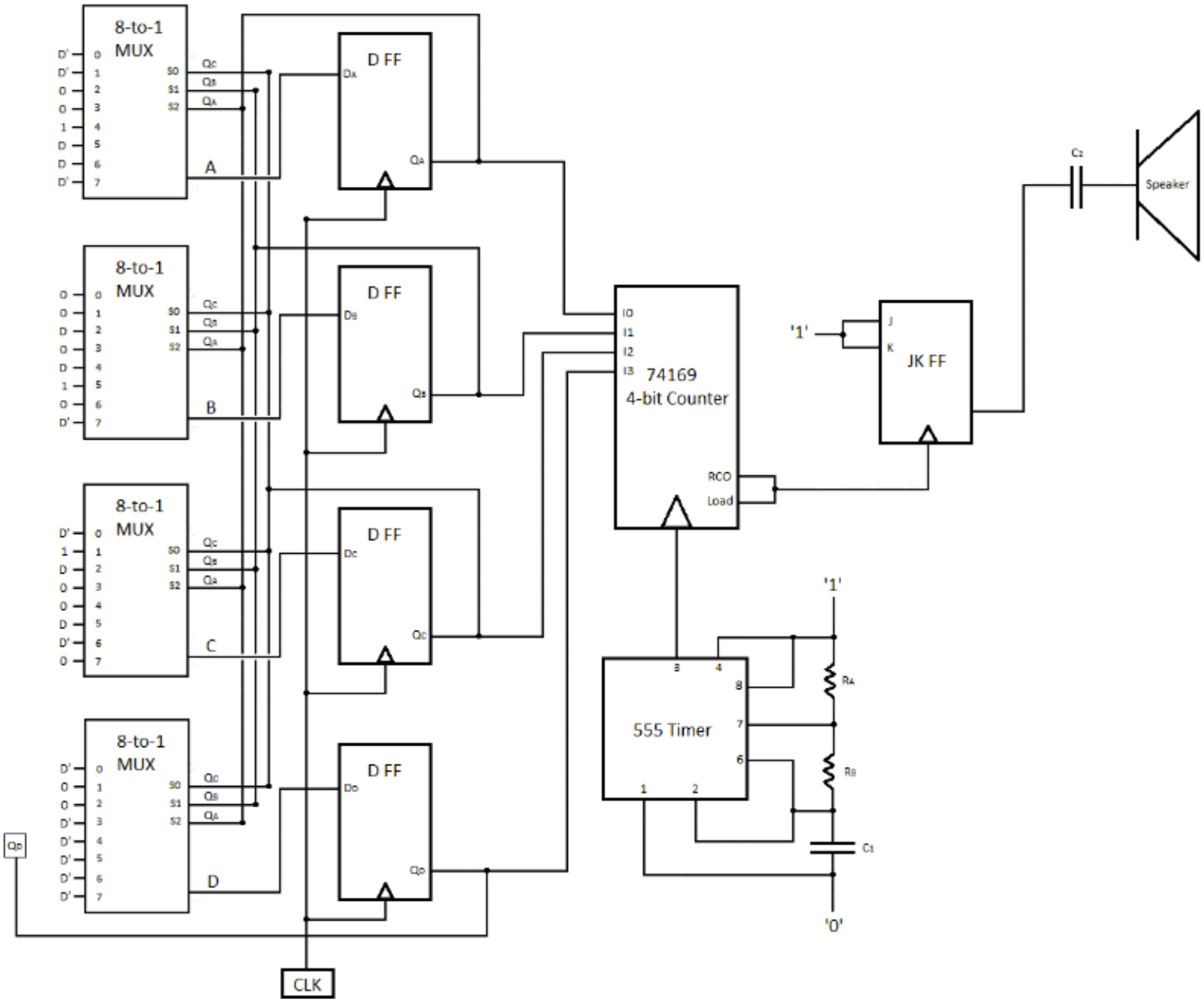
J = T

		Q	
		0	1
T	0	x	0
	1	x	1

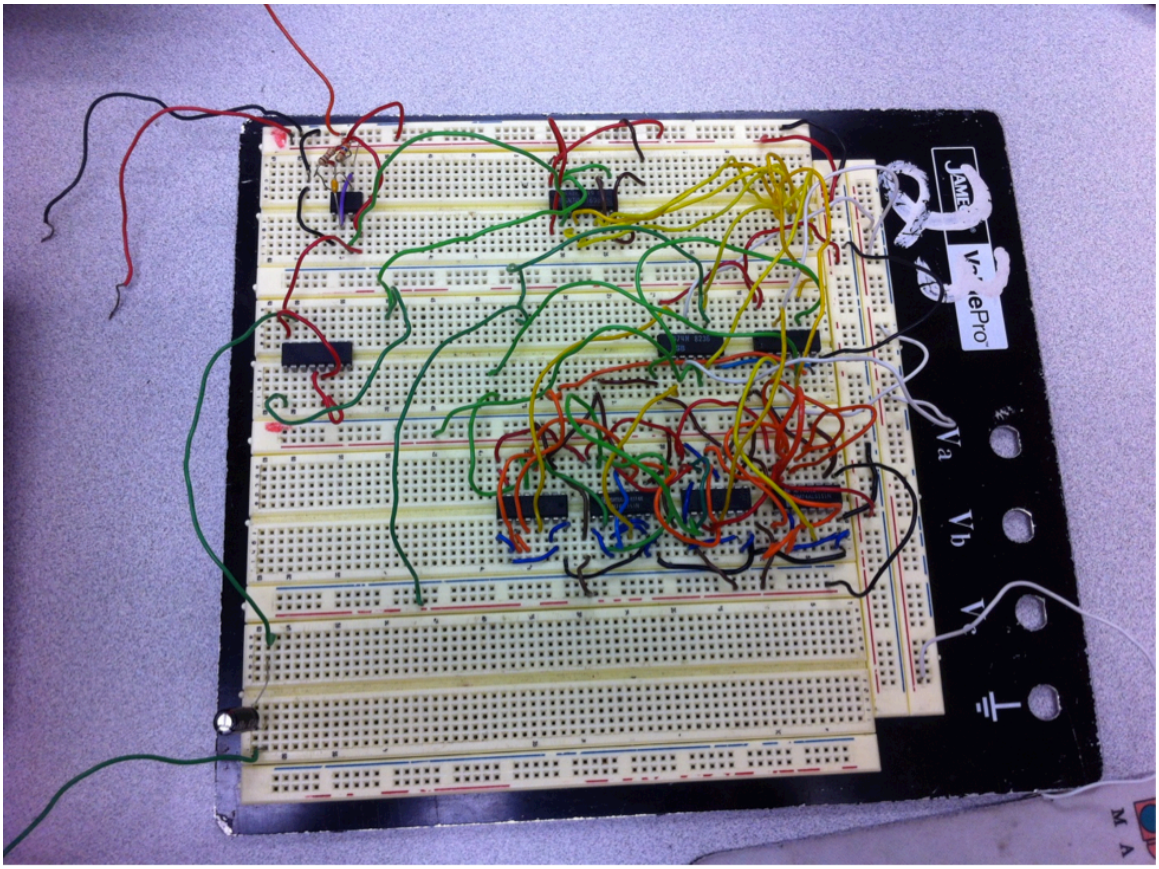
K = T



Complete Logic Diagram



Results and Simulations



Our final circuit. The sequence generator consists of six IC's in the bottom right and the frequency generator consists of the three in the top left. The 555 timer and its connections can be seen in the top left corner.

Answers to the questions in the lab handout

1. *Calculate the maximum frequency at which your circuit can work knowing what chips you have used. Show your calculations and explain them.*

Part of the circuit includes a user-generated clock pulse. Because the circuit component's propagation delays are negligible compared to the frequency of the user input, the circuit's period (and corresponding frequency) will be entirely dependent on the rate at which the user changes the clock pulse.

2. *Calculate the frequency and duty cycle of the signal coming out of the timer according to the resistor and capacitor values you used.*

$$f_0 = \frac{1.44}{(R_A + 2R_B)C} = \frac{1.44}{\big(1.8k\Omega + 2(3.6k\Omega)\big)(10nF)} = 16kHz$$

$$duty\ cycle = \frac{R_A + R_B}{R_A + 2R_B} * 100 = \frac{1.8k\Omega + 3.6\text{k}\Omega}{1.8k\Omega + 2(3.6\text{k}\Omega)} * 100 = 60\%$$

3. *Obtain a formula depending on N for the duty cycle of the RCO output of the frequency divider. Show your equations.*

modulo-N counter with f_0 as CLK produces: $f' = \frac{1}{N+1} * f_0$

JK FF with 50% duty cycle with f' as CLK produces: $f_N = \frac{1}{2} * f'$

$$f_0 = 16kHz$$

$$f_N = \frac{16000}{2N + 2}$$

4. *Assume you have a counter that can only count up. Explain how a modulo-N counting scheme could be implemented.*

Instead of counting up and down, a counter that can only count up would use the $\overline{RCO}$ to output to low when the circuit reaches its maximum state. It would then start counting up again from its initial state.

Conclusion

The circuit produces a different frequency for every state N it counts through. The user may only control the external clock of the flip-flops to cycle through each state. The four outputs of the sequence generator were put into a counter that accepted a 555 timer as its clock. This modulo-n counter would divide the frequency depending on the output of the sequence generator. The output of the counter was put into the clock of a T flip-flop with a 50% duty cycle that accepted logical '1' as its input. This acted to further divide the frequency in half. The final signal was fed into a speaker for playback.

This lab was very effective in demonstrating how 555 timers may be used to generate a frequency and how that frequency can be divided by both a counter and a T flip-flop.

Works Cited

None

Signed OFF

(Included)